PRELIMINARY

PM50RLA060

FLAT-BASE TYPE
INSULATED PACKAGE

Notice : This is not a final specification. Some parametric limits are subject to change.

Pre.	T.Marumo	Rev.	A
Apr.	M.Yamamoto July.5.2002		12-Dec.-'02

PM50RLA060

Feature

a) Adopting new 5th generation IGBT(CSTBT) chip, which performance is improved by 1μm fine rule process.
For example, typical Vce(sat)=1.5V @Tj=125°C

b) I adopt the over-temperature conservation by Tj detection of CSTBT chip, and error output is possible from all each conservation upper and lower arm of IPM.

c) New small package
Reduce the package size by 10%, thickness by 22% from S-DASH series.

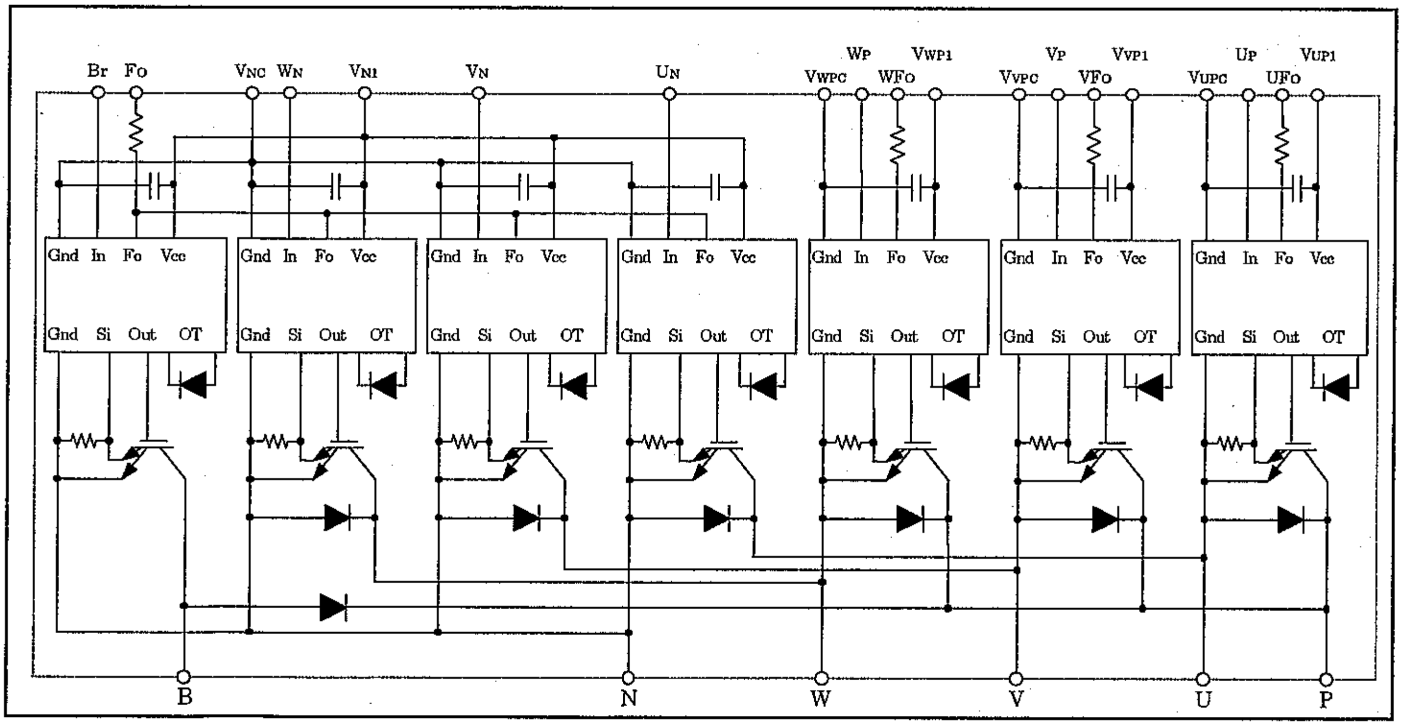
d) Current rating of brake part increased.
60% for the current rating of inverter part.

- 3ϕ 50A, 600V Current-sense IGBT type inverter
- 30A, 600V Current-sense regenerative brake IGBT
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
- Acoustic noise-less 3.7kW class inverter application

OUTLINE DRAWING Dimensions in mm

See Page 7

APPLICATION : General purpose inverter, servo drives and other motor controls



Maximum Ratings (T j = 25°C , unless otherwise noted)

Inverter Part

Item	Symbol	Condition	Ratings	Unit
Collector-Emitter Voltage	V_{CES}	V_D= 15V, V_{CIN}= 15V	600	V
Collector Current	$\pm I_C$	T_C= 25°C	50	A
Collector Current (Peak)	$\pm I_{CP}$	T_C= 25°C	100	A
Collector Dissipation	P_C	T_C= 25°C (Note-1)	134	W
Junction Temperature	Tj		-20 ~ +150	°C

Brake Part

Item	Symbol	Condition	Ratings	Unit
Collector Emitter Voltage	V_{CES}	V_D= 15V, V_{CIN}= 15V	600	V
Collector Current	I_C	T_C= 25°C	30	A
Collector Current (Peak)	I_{CP}	T_C= 25°C	60	A
Collector Dissipation	P_C	T_C= 25°C (Note-1)	79	W
FWDi Rated DC Reverse Voltage	$V_{R(DC)}$	T_C= 25°C	600	V
FWDi Forward Current	I_F	T_C= 25°C	30	A
Junction Temperature	Tj		-20 ~ +150	°C

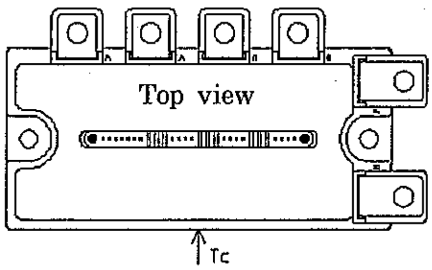
Control Part

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_D	Applied between : V_{UP1}-V_{UPC} V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
Input Voltage	V_{CIN}	Applied between : U_P-V_{UPC}, V_P-V_{VPC} W_P-V_{WPC}, U_N·V_N·W_N·B_r-V_{NC}	20	V
Fault Output Supply Voltage	V_{FO}	Applied betwee : U_{FO}-V_{UPC}, V_{FO}-V_{VPC} W_{FO}-V_{WPC}, F_O-V_{NC}	20	V
Fault Output Current	I_{FO}	Sink current at U_{FO}, V_{FO}, W_{FO}, F_O terminals	20	mA

Total System

Item	Symbol	Condition	Rating	Unit
Supply Voltage Protected by SC	$V_{CC(PROT)}$	V_D= 13.5~16.5V Inverter Part, Tj= +125°C Start	400	V
Supply Voltage (Surge)	$V_{CC(surge)}$	Applied between : P-N , Surge value	550	V
Module Case Operating Temperature	T_C	(Note-1)	-20 ~ +100	°C
Storage Temperature	Tstg		-40 ~ +125	°C
Isolation Voltage	Viso	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	Vrms

(Note-1) Tc(base plate) measurement point is below.



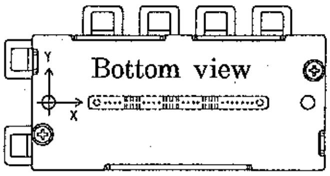
Thermal Resistances

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case Thermal Resistances	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6) (Note-2)	–	–	0.95*	°C/W
	$R_{th(j-c)F}$	Inverter FWDi part (per 1/6) (Note-2)	–	–	1.61*	
	$R_{th(j-c)Q}$	Brake IGBT part (Note-2)	–	–	1.21*	
	$R_{th(j-c)F}$	Brake FWDi part (Note-2)	–	–	2.19*	
	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6) (Note-1)	–	–	1.24	
	$R_{th(j-c)F}$	Inverter FWDi part (per 1/6) (Note-1)	–	–	2.09	
	$R_{th(j-c)Q}$	Brake IGBT part (Note-1)	–	–	1.57	
	$R_{th(j-c)F}$	Brake FWDi part (Note-1)	–	–	2.85	
Contact Thermal Resistance	$R_{th(c-f)}$	Case to fin, (per 1 module) Thermal grease applied (Note-1)	–	–	0.038	

* If you use this value, Rth(f-a) should be measured just under the chips.

(Note-2) Tc(under the chip) measurement point is below. (unit : mm)

axis \ arm	UP		VP		WP		UN		VN		WN		Br	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	29.0	29.5	64.6	65.1	85.9	86.4	38.1	37.6	54.8	55.3	76.1	75.6	18.3	22.4
Y	-7.3	1.6	-7.3	2.1	-7.3	2.1	5.3	-4.6	5.3	-4.6	5.3	-4.6	-7.4	7.0



Electrical Characteristics (Tj= 25°C unless otherwise noted)

Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_D= 15V, V_{CIN}= 0V	Tj= 25°C	–	1.6	2.1	V
		I_C= 50A, Pulsed Fig.1	Tj=125°C	–	1.5	2.0	
FWDi Forward Voltage	V_{EC}	$-I_C$= 50A, V_{CIN}= 15V V_D= 15V Fig.2		–	2.2	3.3	V
Switching Time	ton	V_D= 15V, V_{CIN}= 0V ⟷ 15V		0.5	1.0	2.4	μs
	trr	V_{CC}= 300V, I_C= 50A		–	0.2	0.4	
	tc(on)	Tj= 125°C, Inductive Load		–	0.4	1.0	
	toff	Fig.3		–	1.2	2.5	
	tc(off)			–	0.5	1.0	
Collector-Emitter Cutoff Current	I_{CES}	V_{CE}= V_{CES}	Tj= 25°C	–	–	1	mA
		V_D= 15V Fig.4	Tj=125°C	–	–	10	

Brake Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_D= 15V, V_{CIN}= 0V	Tj= 25°C	–	1.6	2.1	V
		I_C= 30A, Pulsed Fig.1	Tj=125°C	–	1.5	2.0	
FWDi Forward Voltage	V_{FM}	I_F= 30A Fig.2		–	2.2	3.3	V
Collector-Emitter Cutoff Current	I_{CES}	V_{CE}= V_{CES}	Tj= 25°C	–	–	1	mA
		V_D= 15V Fig.4	Tj=125°C	–	–	10	

Control Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit Current	I_D	V_D= 15V	V_{N1}-V_{NC}	–	20	30	mA
		V_{CIN}= 15V	V_{XP1}-V_{XPC}	–	5	10	
Input ON Threshold Voltage	$V_{th(ON)}$	Applied between : U_P-V_{UPC} , V_P-V_{VPC}		1.2	1.5	1.8	V
Input OFF Threshold Voltage	$V_{th(OFF)}$	W_P-V_{WPC} , U_N・V_N・W_N・B_r-V_{NC}		1.7	2.0	2.3	
Short Circuit Trip Level	SC	-20≦Tj≦125°C	Inverter part	100	–	–	A
		V_D=15V Fig.5,6	Brake part	60	–	–	
Short Circuit Current Delay Time	toff(SC)	V_D= 15V Fig.5,6		–	10	–	μs
Over Temperature Protection	OT	Detect T_j of IGBT chip	Trip level	135	145	155	°C
	OTr		Reset level	–	125	–	
Supply Circuit Under-Voltage Protection	UV	-20≦Tj≦125°C	Trip level	11.5	12.0	12.5	V
	UVr		Reset level	–	12.5	–	
Fault Output Current	$I_{FO(H)}$	V_D= 15V, V_{CIN}= 15V		–	–	0.01	mA
	$I_{FO(L)}$	(Note-2)		–	10	15	
Minimum Fault Output Pulse Width	t_{FO}	V_D= 15V (Note-2)		1.0	1.8	–	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

Mechanical Ratings and characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Mounting torque	–	Main terminal screw : M 5	2.5	3.0	3.5	N・m
Mounting torque	–	Mounting part screw : M 5	2.5	3.0	3.5	N・m
Weight	–	–	–	380	–	g

Recommended Conditions For Use

Item	Symbol	Condition	Recommended value	Unit
Supply Voltage	V_{CC}	Applied across P−N terminals	≦ 400	V
Control Supply Voltage	V_D	Applied between : V_{UP1}-V_{UPC} V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC} (Note-3)	15.0±1.5	V
Input ON Voltage	$V_{CIN(ON)}$	Applied between : U_P-V_{UPC}, V_P-V_{VPC}	≦ 0.8	V
Input OFF Voltage	$V_{CIN(OFF)}$	W_P-V_{WPC}, U_N・V_N・W_N・B_r-V_{NC}	≧ 9.0	
PWM Input Frequency	f_{PWM}	Using Application Circuit of Fig.8	≦ 20	kHz
Arm Shoot-through Blocking Time	t_{dead}	For IPM's each input signals Fig.7	≧ 2.0	μs

(Note-3) With ripple satisfying the following conditions
dv/dt swing ≦ ±5V/μs, Variation ≦ 2V peak to peak

Precautions for testing

1. Before appling any control supply voltage (V_D), the input terminals should be pulled up by resistores, etc. to their corresponding supply voltage and each input signal should be kept off state. After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

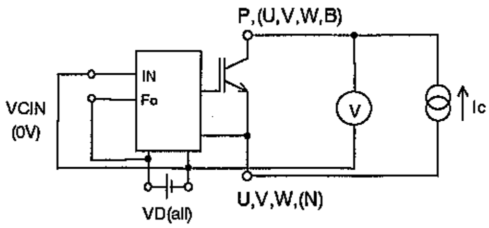


Fig.1 VCE(sat) Tset

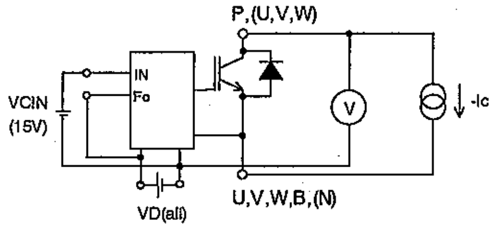


Fig.2 VEC,(VFM) Tset

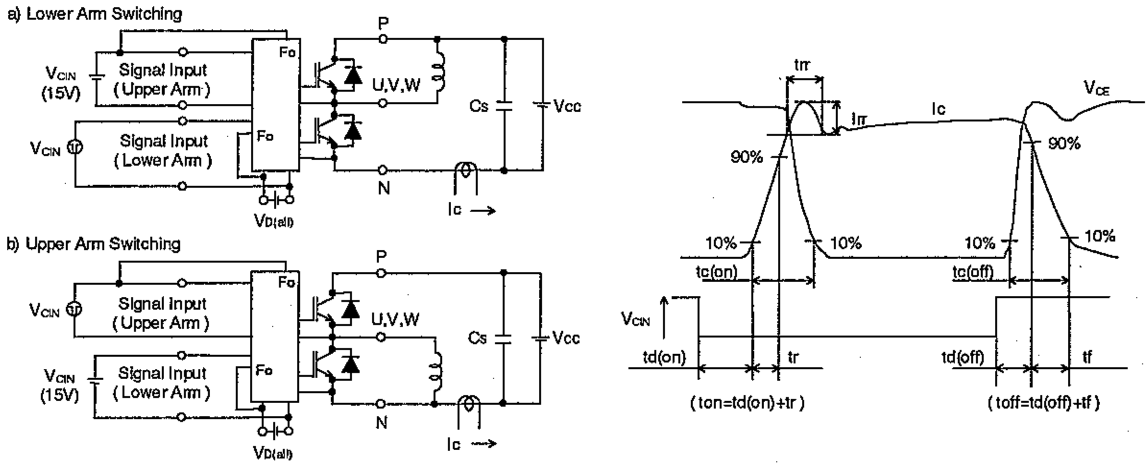


Fig.3 Switching time test circuit and waveform

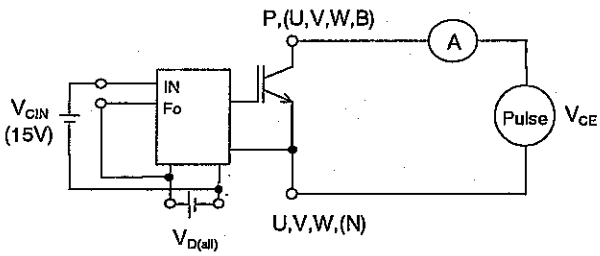


Fig4 ICES Test

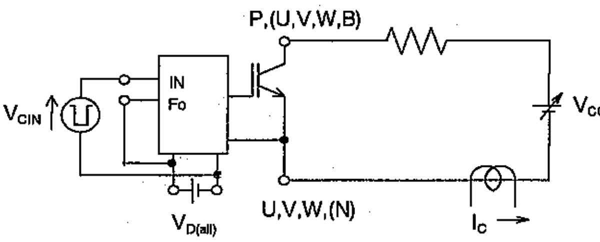


Fig.5 SC Test

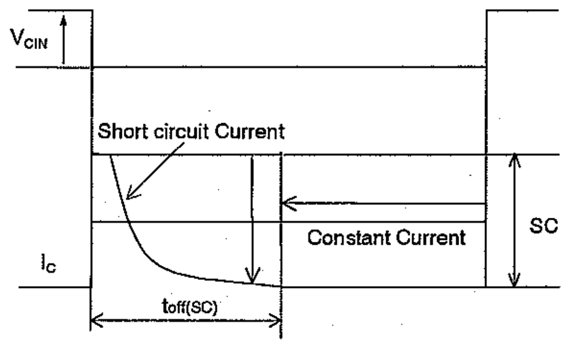
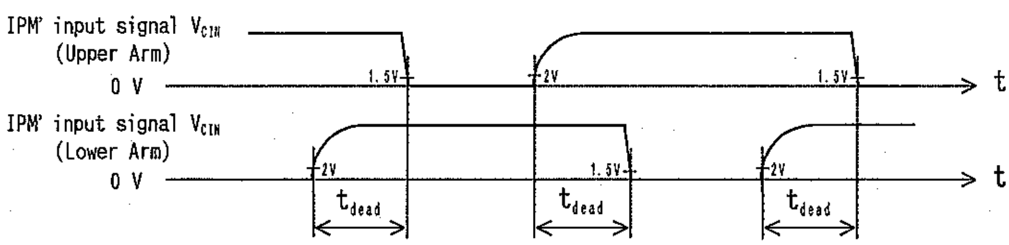
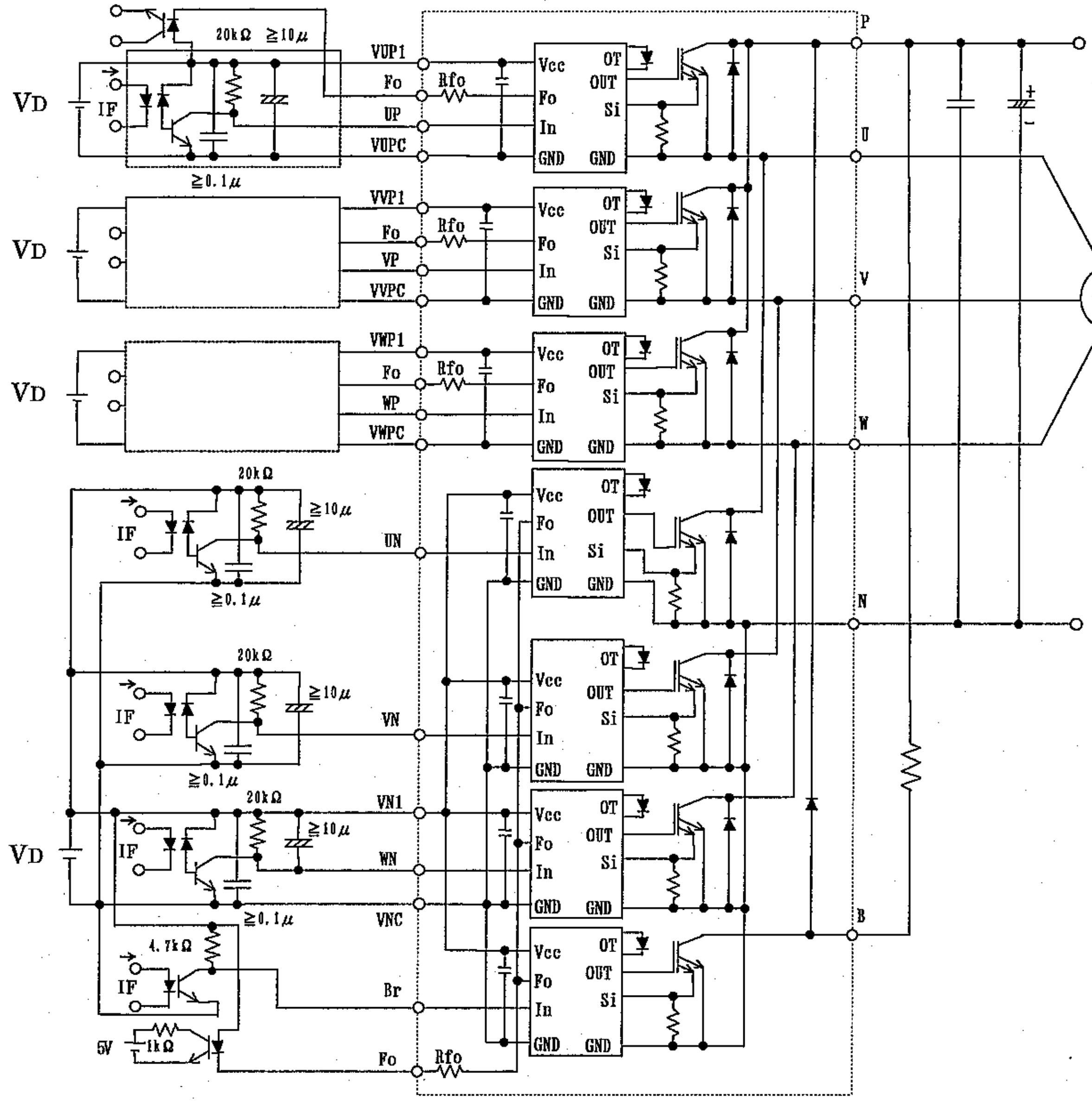


Fig.6 SC Test waveform



1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

Fig.7 Dead time measurement point example



: Interface which is the same as the U-phase

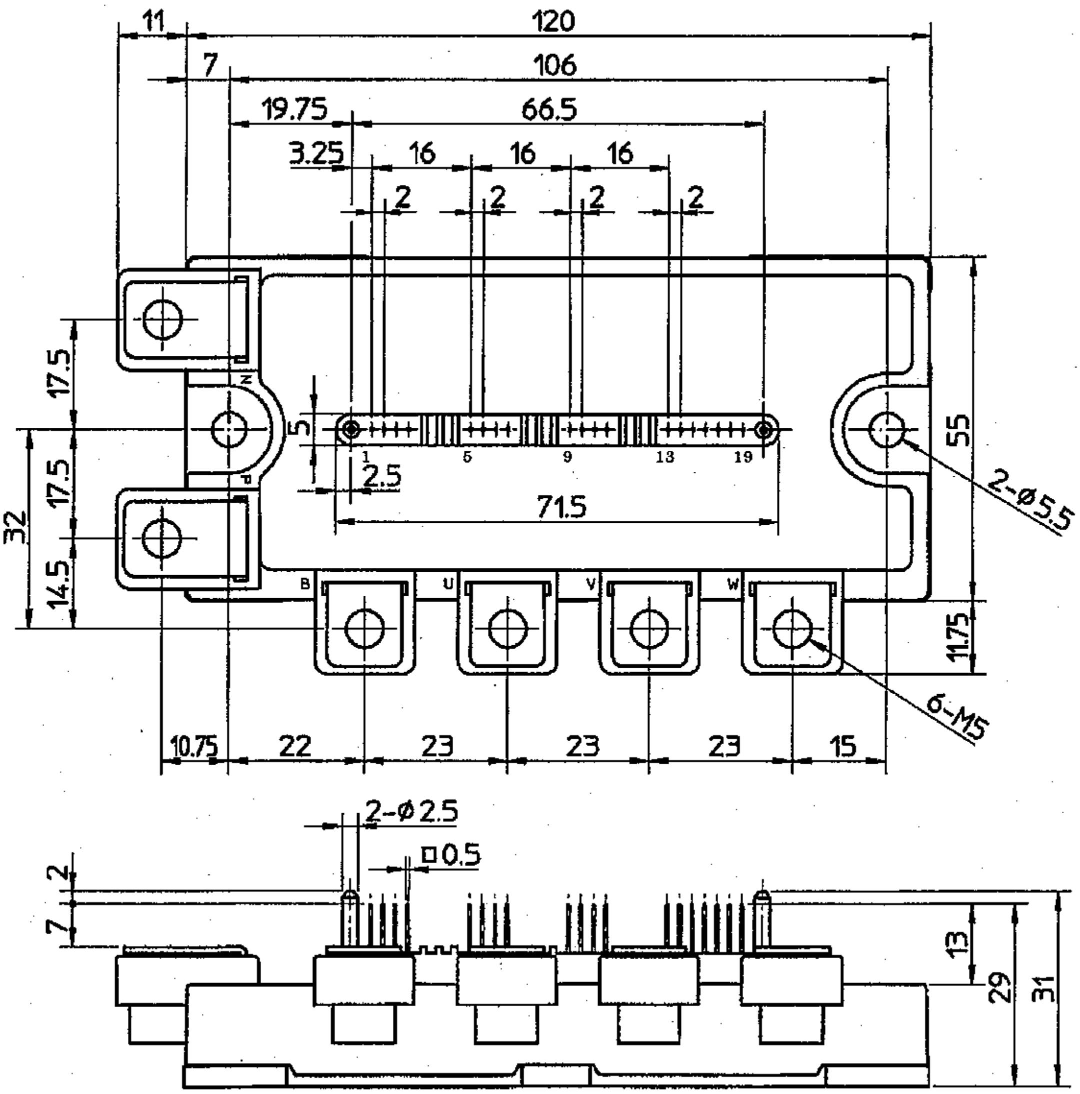
Fig. 8 . Application Example Circuit

Notes for stable and safe operation ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : t_{PLH}, $t_{PHL} \leqq 0.8$ μs, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common -mode noise from AC line and improve noise immunity of the system.

Outline drawings

[Dimensions in mm]



Terminal code

1. VUPC
2. UFO
3. UP
4. VUP1
5. VVPC
6. VFO
7. VP
8. VVP1
9. VWPC
10. WFO
11. WP
12. VWP1
13. VNC
14. VN1
15. Br
16. UN
17. VN
18. WN
19. Fo